AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) An NVRAM fail-over system~~controller~~ comprising:

an~~An~~ NVRAM device ~~connected to a host computer, the host computer having the ability to directly control the NVRAM device~~;

a DMA controller configured to communicate with a host computer and to allow the host computer to program the DMA controller to perform a direct memory transfer between the NVRAM and the host computer; and

an~~An~~ embedded processor coupled to a ~~on the NVRAM fail-over controller that is powered by~~ back-up power supply and to the NVRAM, the processor is configured to communicate with both the NVRAM device and the host computer and to not interfere with the host computer to program the NVRAM.

~~A network interface on the NVRAM fail-over controller that is powered by back-up power.~~

2. (Currently Amended) The system of claim 1, wherein the embedded processor is configured to ~~A method of using a controller of claim 1, the method comprising of the controller performing the following steps:~~

~~the controller determining or being told~~ determine that the host computer has failed[[;]] and to transmit~~ting~~ NVRAM data to a second~~another~~ computer via a network interface.

3. (Currently Amended) The system of claim 1, wherein the embedded processor is configured to ~~A method of using a controller of claim 1, the method comprising of the controller performing the following steps:~~

~~the controller determining or being told~~ determine that the host computer has failed[[;]] and to respond~~ing~~ to requests from another computer to transmit part or all of the NVRAM data via a network interface.

4. (Cancelled).

5. (Currently Amended) The system of claim 1, further comprising: ~~A controller of claim 1 using~~ a non-transparent bus bridge[[s]] configured to transfer information between the host computer and the DMA controller.

6. (Currently Amended) The system of claim 5, wherein the non-transparent bus bridge ~~A method of using a controller of claim 5 in which the bridges~~ acts as a firewall[[s]] to protect one portion of the NVRAM fail-over system from failures on ~~the other~~ a host computer side of the firewall~~, the method comprising of the controller performing the following steps:~~, wherein the embedded processor is configured to program the non-transparent bus bridge to either forward or not to forward data from the host computer based on an operating status of the host computer.

~~the controller determining or being told that the host computer has failed;~~

~~the controller programming its bridge between itself and the host computer to not forward requests through the bridge;~~

~~the controller continuing its operations including transmission or storage of NVRAM data;~~

~~the controller receiving a network message that it is OK to reestablish a connection through the bridge or the host computer proving itself healthy enough to reprogram the bridge.~~

7. (Cancelled)

8. (Currently Amended) The system ~~A controller~~ of claim 1, further comprising an interface configured to connect with a ~~the ability to add~~ daughter card[[s]].

9. (Currently Amended) The system ~~A controller~~ of claim 8, wherein ~~in which~~ the daughter card is a network controller under control of the host computer.

10. (Currently Amended) The system ~~A controller~~ of claim 8, wherein ~~in which~~ the daughter card is a disk or RAID controller under control of the host computer.

11. (Currently Amended) The system ~~A controller~~ of claim 8, wherein ~~in which~~ the daughter card is a disk or RAID controller under control of the embedded processor.

12. (Currently Amended) The system of claim 10, wherein the ~~A controller of claims 10 or 11 used as a~~ embedded processor is configured to operate as a RAID controller for ~~device with NVRAM under control of~~ the host computer along with the daughter card.

13. (Currently Amended) The system ~~A controller~~ of claim 1, wherein the embedded processor is configured to ~~used as an NVRAM device that~~ preserve[[s]] data stored in the NVRAM during long outages by sending the stored data~~it~~ to a second~~another~~ host computer coupled to a network interface~~over a network or to a disk attached as in claims 10 or 11~~, thereby allowing the NVRAM to retrieve ~~and that retrieves~~ such data back ~~into NVRAM~~ at a later time.

14. (Currently Amended) The system ~~A controller~~ of claim 1, wherein the embedded processor is configured to allow ~~used as an NVRAM device that preserves data during long outages by sending it to another computer over a network such that the other~~ a second computer ~~can~~ to take over operations from the ~~first~~ host computer in communication with the DMA controller, thereby~~such as~~ managing storage devices and using network addresses of ~~from~~ the host computer.

15. (Currently Amended) The system of claim 1, wherein the embedded processor is configured to perform the following operations: ~~A method as in claims 11 or 12 that further keeps the remote server system almost up-to-date during normal operation to reduce the time to bring it fully up-to-date when a failure occurs, such method comprising of the controller performing the following steps:~~

~~receiving data in NVRAM from the host computer;~~

inform~~telling~~ the host computer that ~~the~~ a data transfer to the NVRAM is complete;

inform~~ing~~ a second~~another~~ computer that the data stored in the NVRAM is available;

transfer~~ing~~ data to the second~~other~~ computer at a suitable time;

keep~~ing~~ track of what data still remains to be sent;

and ~~at a later time~~

~~the controller determining or being told that the host computer has failed;~~

transfering all unsent data to the second~~other~~ computer after the host computer failed.

16. (Currently Amended) The system ~~A controller~~ of claim 1, further comprising ~~with~~ a watchdog timer to reset the embedded processor.

17. (Currently Amended) The system ~~A controller~~ of claim 1, wherein the embedded processor is configured to allow ~~with the ability for~~ the host computer to reset the embedded processor.

18. (New) The system of claim 10, wherein the embedded processor is configured to preserve data stored in the NVRAM during long outages by sending the stored data to the disk coupled to the interface of the daughter card.

19. (New) The system of claim 11, wherein the embedded processor is configured to operate as a RAID controller for host computer.

20. (New) The system of claim 11, wherein the embedded processor is configured to preserve data stored in the NVRAM during long outages by sending the stored data to the disk coupled to the interface of the daughter card.

21. (New) The system of claim 1, further comprising:

a bus interface configured to communicate with the host computer;

a non-transparent bus bridge having a first I/O interface and a second I/O interface, the first I/O interface being coupled to the embedded processor and the second I/O interface being coupled to the NVRAM device and to the bus interface, thereby allowing the host computer to communicate directly with the NVRAM device without passing data between the first and second I/O interfaces, wherein the non-transparent bus bridge is configured to act as a firewall

between the first and second I/O interfaces to protect the host computer from failures the first I/O interface side of the firewall by allowing the host computer to program the non-transparent bus bridge to either forward or not to forward data through the non-transparent bus bridge